WHAT IS CLAIMED IS:

1. A device for estimating the number of board layers constituting a board, which is connected to at least one file for storing information about an order of layers to be added, positional information of a component pin, a board pin, a power-source pin, and a ground pin, connection information between a component pin and a board pin, connection information between a power-source pin or a ground pin and a predetermined layer, information about existing wirings, information about an area where wiring is prohibited, and information about a shape of a via, a storage and an output device to which a wired result is output, comprising:

a layer adding section for retrieving from the file the information about an order of layers to be added to form an original layer structure and to store information about the formed original layer structure in the storage;

a via forming section for retrieving from the file positional information of a component pin, a board pin, a power-source pin, and a ground pin, and connection information between a component pin and a board pin to store the information in the storage, and retrieving from the file the connection information from a power-source pin or ground pin to a predetermined layer and the information about a shape of a via to form a via and to store the information and information about the formed via with its shape in the storage;

a wiring prohibited area forming section for retrieving from the file the information about existing wirings and the information about an area where wiring is prohibited to store the information in the storage; and

a wiring route searching section for searching for a wiring route in reference to the information stored in the storage to output to the output device a structure of a present board and the number of layers

constituting the present board.

2. A device for estimating the number of board layers constituting a board, as claimed in claim 1, wherein;

the file further stores connection information between a component pin group composed of a plurality of component pins and a board pin group composed of a plurality of board pins;

the via forming section retrieves from the file the connection information between the component pin group and the board pin group to store the information in the storage, and retrieves from the file the connection information between a power-source pin or ground pin and a predetermined layer and the information about a shape of a via to form a via and to store the information and information about the formed via with its shape in the storage; and

the wiring route searching section outputs to the output device net assignment information indicating a connection between two pins in the component pin group and the board pin group, respectively, in addition to the structure of the present board and the number of board layers constituting the present board, wherein:

the two pins are arbitrarily selected from the component pin group and the board pin group, respectively.

3. A device for estimating the number of board layers constituting a board as claimed in claim 1, wherein:

the wiring route searching section calculates a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching section outputs to the output device the structure of the present board and the number of board layers constituting the present board; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding section retrieves from the file the information about an order of layers to be added to store the information in the storage.

4. A device for estimating the number of board layers constituting a board as claimed in claim 2, wherein:

the wiring route searching section calculates a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching section outputs to the output device the structure of the present board, the number of board layers constituting the present board, and the net assignment information; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding section retrieves from the file the information about an order of layers to be added to store the information in the storage.

5. A system for estimating the number of board layers constituting a board, comprising:

at least one file for storing information about an order of layers to be added, positional information of a component pin, a board pin, a power-source pin, and a ground pin, connection information between a component pin and a board pin, connection information between a power-source pin or a ground pin and a predetermined layer, information about existing wirings, information about an area where wiring is prohibited, and information about a shape of a via;

a storage;

an output device to which a wired result is output; and

a device for estimating the number of board layers constituting

a board as claimed in any one of claims 1 to 4, wherein:

the device for estimating the number of board layers constituting a board comprises:

a layer adding section for retrieving from the file the information about an order of layers to be added to form an original layer structure and to store information about the formed original layer structure in the storage;

a via forming section for retrieving from the file positional information of a component pin, a board pin, a power-source pin, and a ground pin, and connection information between a component pin and a board pin to store the information in the storage, and retrieving from the file the connection information from a power-source pin or ground pin to a predetermined layer and the information about a shape of a via to form a via and to store the information and information about the formed via with its shape in the storage;

a wiring prohibited area forming section for retrieving from the file the information about existing wirings and the information about an area where wiring is prohibited to store the information in the storage; and

a wiring route searching section for searching for a wiring route in reference to the information stored in the storage to output to the output device a structure of a present board and the number of layers constituting the present board.

6. A system for estimating the number of board layers constituting a board, as claimed in claim 5, wherein;

the file further stores connection information between a component pin group composed of a plurality of component pins and a board pin group composed of a plurality of board pins;

the via forming section retrieves from the file the connection

information between the component pin group and the board pin group to store the information in the storage, and retrieves from the file the connection information between a power-source pin or ground pin and a predetermined layer and the information about a shape of a via to form a via and to store the information and information about the formed via with its shape in the storage; and

the wiring route searching section outputs to the output device net assignment information indicating a connection between two pins in the component pin group and the board pin group, respectively, in addition to the structure of the present board and the number of board layers constituting the present board, wherein:

the two pins are arbitrarily selected from the component pin group and the board pin group, respectively.

7. A system for estimating the number of board layers constituting a board as claimed in claim 5, wherein:

the wiring route searching section calculates a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching section outputs to the output device the structure of the present board and the number of board layers constituting the present board; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding section retrieves from the file the information about an order of layers to be added to store the information in the storage.

8. A system for estimating the number of board layers constituting a board as claimed in claim 6, wherein:

the wiring route searching section calculates a securement

ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching section outputs to the output device the structure of the present board, the number of board layers constituting the present board, and the net assignment information; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding section retrieves from the file the information about an order of layers to be added to store the information in the storage.

9. A method for estimating the number of board layers constituting a board and outputting a wired result, comprising:

a layer adding step for retrieving information about an order of layers to be added, the information being stored in at least one file, to store the information in a storage;

a via forming step for retrieving positional information of a component pin, a board pin, a power-source pin, and a ground pin and connection information between a component pin and a board pin, the information being stored in the file, to store the information in the storage, and retrieving connection information from a power-source pin or ground pin to a predetermined layer and information about a shape of a via, the information being stored in the file, to form a via and to store the information and information about the formed via with its shape in the storage;

a wiring prohibited area forming step for retrieving information about existing wirings and information about an area where wiring is prohibited, the information being stored in the file, to store the information in the storage; and

a wiring route searching step for searching a wiring route in reference to the information stored in the storage to output to an output

device a structure of a present board and the number of layers constituting the present board.

10. A method for estimating the number of board layers constituting a board and outputting a wired result, as claimed in claim 9, wherein:

the via forming step further comprises a step of retrieving connection information between a component pin group composed of a plurality of component pins and a board pin group composed of a plurality of board pins, the information being stored in the file, to store the information in the storage, and retrieving the connection information between a power-source pin or ground pin and a predetermined layer and the information about a shape of a via to form a via and to store the information and information about the formed via with its shape in the storage; and

the wiring route searching step further comprises a step of outputting to the output device net assignment information indicating a connection between two pins in the component pin group and the board pin group, respectively, in addition to the structure of the present board and the number of board layers constituting the present board, wherein:

the two pins are arbitrarily selected from the component pin group and the board pin group, respectively.

11. A method for estimating the number of board layers constituting a board and outputting a wired result as claimed in claim 9, wherein:

the wiring route searching step further comprises a step of calculating a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching step further comprises a step of outputting to

the output device the structure of the present board and the number of board layers constituting the present board; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding step further comprises a step of retrieving from the file the information about an order of layers to be added to store the information in the storage.

12. A method for estimating the number of board layers constituting a board and outputting a wired result as claimed in claim 10, wherein:

the wiring route searching step further comprises a step of calculating a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching step further comprises a step of outputting to the output device the structure of the present board, the number of board layers constituting the present board, and the net assignment information; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding step further comprises a step of retrieving from the file the information about an order of layers to be added to store the information in the storage.

13. A program for estimating the number of board layers constituting a board and outputting a wired result, to have a computer execute:

a layer adding process for retrieving information about an order of layers to be added, the information being stored in at least one file, to store the information in a storage;

a via forming process for retrieving positional information of a component pin, a board pin, a power-source pin, and a ground pin and

connection information between a component pin and a board pin, the information being stored in the file, to store the information in the storage, and retrieving connection information from a power-source pin or ground pin to a predetermined layer and information about a shape of a via, the information being stored in the file, to form a via and to store the information and information about the formed via with its shape in the storage;

a wiring prohibited area forming process for retrieving information about existing wirings and information about an area where wiring is prohibited, the information being stored in the file, to store the information in the storage; and

a wiring route searching process for searching a wiring route in reference to the information stored in the storage to output to an output device a structure of a present board and the number of layers constituting the present board.

14. A program for estimating the number of board layers constituting a board and outputting a wired result, as claimed in claim 13, wherein:

the via forming process further comprises a process for retrieving connection information between a component pin group composed of a plurality of component pins and a board pin group composed of a plurality of board pins, the information being stored in the file, to store the information in the storage, and retrieving the connection information between a power-source pin or ground pin and a predetermined layer and the information about a shape of a via to form a via and to store the information and information about the formed via with its shape in the storage; and

the wiring route searching process further comprises a process for outputting to the output device net assignment information indicating

a connection between two pins in the component pin group and the board pin group, respectively, in addition to the structure of the present board and the number of board layers constituting the present board, wherein:

the two pins are arbitrarily selected from the component pin group and the board pin group, respectively.

15. A program for estimating the number of board layers constituting a board and outputting a wired result as claimed in claim 13, wherein:

the wiring route searching process further comprises a process for calculating a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching process further comprises a process for outputting to the output device the structure of the present board and the number of board layers constituting the present board; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding process further comprises a process for retrieving from the file the information about an order of layers to be added to store the information in the storage.

16. A program for estimating the number of board layers constituting a board and outputting a wired result as claimed in claim 14, wherein:

the wiring route searching process further comprises a process for calculating a securement ratio for the wiring route; and

when 100 % securement ratio for the wiring route is obtained, the wiring route searching process further comprises a process for outputting to the output device the structure of the present board, the number of board layers constituting the present board, and the net assignment information; or

when 100 % securement ratio for the wiring route is not obtained, the layer adding process further comprises a process for retrieving from the file the information about an order of layers to be added to store the information in the storage.